III. Amendments to the Specification

Please amend Paragraph 29 as follows:

[0029] As noted above, the bit switch path can be turned off for a programmed cell or I/O by signal PD[n] coupled to the control gate of PMOS QPL. Each signal PD is the inverse state of the respective signal PDN and its logical high is set to VDQ2 and logical low to VSS.

Please amend Paragraph 30 as follows:

[0030] The memory circuit of FIG. 5, although not shown, may still include a leakage path from node VDQ2 to ground as shown in FIG. 2 to reduce any initial overshoot of VDQ2 discussed above in connection with FIG. 2. This current, however, will be mirrored in circuit 200 by the ~~cell~~ bit line current detector PMOS QP1. The effect of this leakage current can be neutralized by turning on the leakage current circuit for a time interval, for example, 1 μs, to stabilize the VDQ2 level and turning off the leakage current circuit thereafter. A timing circuit (not shown) may be used to control this time duration. The timer that generates control signals for the timing of program pulses, overerase pulses and erase pulses may be used. During this interval, the input to the differential amplifier 122 can be set to VR rather than VRP, essentially disconnecting Detector and Tuner Circuit 200 from differential amplifier 122 and setting VDQ2 to a constant voltage. After this time interval, VRP is connected to the differential amplifier and, optionally, a small leakage path circuit can be turned on to replace the original leakage path circuit for avoiding VDQ2 overshoot. The leakage path circuit may comprise, as one of ordinary skill familiar with the prior art circuit of FIG. 2 will recognize, one or more NMOS transistors coupled in series to node VDQ2. If the voltage at VDQ2 is too high, the current will sink through the NMOS transistors to ground. Once the VDQ2 level is stabilized, the leakage current can be reduced by connecting smaller NMOS transistors to node VDQ2.

Please amend Paragraph 33 as follows:

[0033] Tables 2-1 and 2-2 below illustrate the results of a software simulation of the circuit of FIG. 6, with resistors used to simulate the bit switch resistances. The tables illustrate two conditions – (1) there is only one erased cell to be programmed, or one bit line to be overerase corrected, and (2) there are eight erased cells to be programmed or eight bit lines to be overerase corrected. Tables 2-1 and 2-2 illustrate that the VBL difference when total bit line current is increased is reduced by the change in VRP, and thus VDQ2, as the total bit line current is increased or decreased. The simulation illustrates that the change in VBL due to changes in bit line current is less than or equal to about 0.17 volts for each simulation. The simulation assumed that the temperature coefficient of resistance of Rt is 1000 ppm/°C ~~ppm/0°C~~. The "VBL" voltage in the chart shows the bit line voltage on a bit line with non-zero bit line current (i.e., on a bit line being programmed or overerase corrected) and for the bit line with zero bit line current and QPL "on".[[.]] The VBL voltage will be VDQ2 for the bit line with zero bit line current and QPL "on".

Please amend Paragraph 34 as follows:

[0034] Tables 3-1 and 3-2 below illustrate the results of a software simulation of the circuit of FIG. 6, only using transistors to simulate the bit switch resistances. The tables illustrate two conditions – (1) there is only one erased cell to be programmed, or one bit line to be overerase corrected, and (2) there are eight erased cells to be programmed or eight bit lines to be overerase corrected. Tables 3-1 and 3-2 indicate results that are similar to Tables 2-1 and 2-2 in that VBL stays relatively constant (i.e., the largest change in VBL due to a change in total bit line current was only about 0.2V). The simulation assumed that the temperature coefficient of resistance of Rt is 1000 ppm/°C ~~ppm/0°C~~.